PENDING CLAIMS:

1. (Original) An integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the processor; and

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps,

wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface.

2. (Previously Presented) An integrated circuit according to claim 1, which comprises a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

3. (Original) An integrated circuit according to claim 1, wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

4. (Original) An integrated circuit according to claim 3, wherein said switching means comprises a multiplexer.

5. (Original) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory mapped peripheral.

6. (Original) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

7. (Original) An integrated circuit according to claim 1, which comprises control registers addressable in said memory space, wherein in said first memory address map said first range of addresses include addresses of control registers associated with said at least one resource and in said second address map said addresses are reallocated to control registers associated with the interface.

8. (Original) An integrated circuit according to claim 2, wherein said mode is set by application of a logic value selected from one and zero on the mode setting pin.

9. (Original) An integrated circuit according to claim 1, wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

10. (Original) An integrated circuit according to claim 9, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

11. (Original) An integrated circuit according to claim 10, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

12. (Original) A prototype system comprising an integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the, processor;

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in the second memory address map said first range of addresses are also allocated to the interface; and

an off-chip circuit connected to said interface and including at least one off-chip memory resource.

13. (Previously Presented) A prototype system according to claim 12, which comprises a mode setting pin operatively connected to the request directing unit for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

14. (Original) A prototype system according to claim 12, wherein said request directing unit comprises switching circuitry responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

15. (Original) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory mapped peripheral.

16. (Original) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

17. (Original) A prototype system according to claim 12, wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

18. (Original) A prototype system according to claim 17, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

19. (Original) A prototype system according to claim 12, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

20. (Original) A method of evaluating a prototype system comprising an integrated circuit including an on-chip processor associated with at least one on-chip memory resource and an off-chip circuit associated with at least one off-chip memory resource, the method comprising:

executing a computer program on the on-chip processor, said program causing the generation of memory access requests, each memory access request including an address identifying an address in memory to which the request is directed; and

in accordance with a selected mode of operation, selectively supplying said memory access requests to at least one of said first and second memory address maps, and directing the memory access requests selectively to said on-chip memory resource or said off-chip circuit in dependence on the selected one of said first and second address maps.

21. (Original) A method according to claim 20, wherein said mode of operation is selected by application of selectable logic values to a mode setting pin.

22. (Original) A method according to claim 20, wherein said memory access requests are directed off-chip via an interface whose address space replaces the address space of the on-chip memory resource in the second memory address map.

23. (Original) A method according to claim 22, wherein said memory access requests take the form of packets.

24. (Original) A method according to claim 23, wherein packets are chopped into chunks and transmitted in a plurality of cycles when being conveyed off-chip.

25. (Original) A method according to claim 23, wherein chunks received in a plurality of cycles from the off-chip circuit are reassembled into packets for transmission on-chip.

26. (Original) An integrated circuit comprising: processing means operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed; at least one on-chip resource falling within the address space addressable by the processing means; interface means for directing packets off-chip and addressable within the address space of the processing means; and means for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface and in the second address map the first range of addresses are also allocated to the interface.